SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH DUAL INSULATION SYSTEM

Field of the Invention

The present invention relates to a semiconductor integrated circuit device and, more particularly, to a semiconductor integrated circuit device using a power supply voltage and other operation voltages such as a higher voltage than the power supply voltage.

Background of the Invention

Electronic apparatuses such as a personal digital assistant (PDA), a notebook computer or a mobile phone operate with a power supplied from a battery. Users want to use such these electronic apparatuses for longer time without recharge, which can be achieved by lowering operation current or voltage. In addition, state-of-the-art electronic apparatuses require higher operation speed. In order to achieve higher speed, a gate insulation layer of a MOS transistor must be formed more thinly.

An electronic apparatus operating with a lower operation voltage includes a number of semiconductor integrated circuit devices. Each of the semiconductor integrated circuit devices uses an external power supply voltage as an internal power supply voltage as well as a higher voltage than the external or internal power supply voltage. A relatively thick insulation layer is adapted in a MOS transistor operating with a high voltage so as to enhance a withstanding voltage relative to the high voltage. On the other hand, a relatively thin insulation layer is adapted in a MOS transistor

operating with a lower voltage than the high voltage. Such an insulation system is called "dual insulation system".

In the case that a relatively thick insulation layer is adapted, it is possible to prevent the gate insulation layer from being broken due to a gate-drain voltage difference of a MOS transistor. The greater the gate insulation layer is, the higher a threshold voltage of the MOS transistor becomes. When the threshold voltage of the MOS transistor becomes higher, a turn-on speed of the MOS transistor may be lowered. Thus, an entire operation speed may be lowered. As a result, what is required is a control technique to overcome the above-mentioned disadvantages.

Summary of the Invention

In view of the foregoing, the present invention provides a semiconductor integrated circuit device which prevents an operation speed from being lowered in a dual insulation system.

Further, the present invention provides a semiconductor integrated circuit device which efficiently reduces an electric field applied to a gate insulation layer of a MOS transistor in a dual insulation system.

According to an aspect of the present invention, a semiconductor integrated circuit device comprises a first internal circuit including a first MOS transistor operating with a first voltage higher than a power supply voltage and having a relatively thick gate insulation layer; a second internal circuit including a second MOS transistor operating with a second voltage lower than the first voltage and having a relatively thin gate insulation layer; and restricting means for restricting a voltage transmitted from the first internal circuit to the second internal voltage so as to reduce an electric filed

applied to the gate insulation layer of the second MOS transistor.

The second voltage is one of an external power supply voltage, the power supply voltage, a voltage lower than the power supply voltage, and a voltage higher than the power supply voltage and lower than the first voltage. The restricting means includes a third MOS transistor operating with the second voltage and having the relatively thin gate insulation layer. More specifically, a voltage from the first internal voltage is applied to the second internal circuit through the third MOS transistor.

According to another aspect of the invention, a semiconductor integrated circuit device comprises a power terminal receiving a high voltage higher than a power supply voltage; a first transistor having a first current electrode coupled to the power terminal, a second current electrode coupled to an output terminal, and a gate coupled to a first input signal; a second transistor having a first current electrode coupled to the output terminal, a second current electrode, and a gate coupled to a low voltage lower than the high voltage; and a third transistor having a first current electrode coupled to the second current electrode of the second transistor, a second current electrode coupled to a ground voltage, a gate connected to receive a second input signal. The first transistor has a relatively thick gate insulation layer. Each of the second and third transistors has a relatively thin gate insulation layer.

In a preferred embodiment, the low voltage is one of external power supply voltage, the power supply voltage, a voltage lower than the power supply voltage, a voltage higher than the power supply voltage and lower than the high voltage.

In a preferred embodiment, the first input signal selectively has a

high level of the first voltage and a low level of the ground voltage.

In a preferred embodiment, the second input signal selectively has a high level of the low voltage and a low level of the ground voltage.

In a preferred embodiment, the second input signal includes a row address signal in a semiconductor memory device.

In a preferred embodiment, the semiconductor integrated circuit device further comprises an inverter coupled to a connection node of the second and third transistors. The inverter drives a wordline of the semiconductor memory device. The inverter includes PMOS and NMOS transistors operating with the high voltage and each having the relatively thick gate insulation layer.

In a preferred embodiment, the semiconductor integrated circuit device further comprising a fourth transistor coupled between the third transistor and the ground voltage. The fourth transistor has the relatively thin gate insulation layer. The fourth transistor is controlled by a block selecting signal in a semiconductor memory device.

According to still another aspect of the invention, a semiconductor integrated circuit device comprises a power terminal receiving a high voltage higher than a power supply voltage; a first MOS transistor having a relatively thick gate insulation layer, the first MOS transistor being coupled between the power terminal and a first internal node; a second MOS transistor having the relatively thick gate insulation layer, the second MOS transistor being coupled between the power terminal and a second internal node, wherein the first MOS transistor is controlled by a voltage of the second internal node, and the second MOS transistor is controlled by a voltage of the first internal node; third and fourth MOS transistors each

having a relatively thin gate insulation layer, the third MOS transistor being coupled between the first internal node and a third internal node and the fourth MOS transistor being coupled between the second internal node and a fourth internal node; and fifth and sixth MOS transistors each having the relatively thin gate insulation layer, the fifth MOS transistor being coupled between the third internal node and a ground voltage and the sixth MOS transistor being coupled between the fourth internal node and the ground voltage. Gates of the third and fourth MOS transistors are coupled to a low voltage lower than the high voltage. The fifth MOS transistor is controlled by a first input signal, and the sixth MOS transistor is controlled by an inverted version of the first input signal.

In a preferred embodiment, the first input signal and its inverted version selectively have a high level of the low voltage and a low level of the ground voltage, respectively. The low voltage is one of an external power supply voltage, the power supply voltage, a voltage lower than the power supply voltage, and a voltage higher than the power supply voltage and lower than the high voltage.

In a preferred embodiment, the first input signal includes a row address signal and a block selecting signal in a semiconductor memory device.

In a preferred embodiment, the first internal node is coupled to a row decoder and driver block of the semiconductor memory device, and the row decoder and driver block selectively drives wordlines of the semiconductor memory device in response to row address signals.

In a preferred embodiment, the row decoder and driver block includes row decoder and driver circuits each corresponding to wordlines. Each of the

row decoder and driver circuits includes a seventh MOS transistor having a source coupled to the high voltage, a drain coupled to a fifth internal node, and a gate connected to receive a second input signal; and eighth and ninth MOS transistors serially coupled between the fifth internal node and the ground voltage. Each of the seventh and eighth MOS transistors has the relatively thick gate insulation layer, and the ninth MOS transistor has the relatively thin gate insulation layer. The eighth MOS transistor is controlled by a voltage of the first internal node.

Brief Description of the Drawings

FIG. 1 is a circuit diagram of a semiconductor integrated circuit device according to the present invention.

FIG. 2 is a diagram for explaining a difference between voltages applied to a gate insulation layer in a MOS transistor shown in FIG. 1.

FIG. 3 and FIG. 4 are circuit diagrams showing other embodiments of semiconductor integrated circuit devices according to the present invention.

FIG. 5 is a block diagram of a semiconductor memory device using the semiconductor integrated circuit device according to the present invention.

FIG. 6 is a circuit diagram showing a portion of a level shift block shown in FIG. 5.

FIG. 7 is a circuit diagram showing a portion of a row decoder & driving block shown in FIG. 5.

FIG. 8 is a timing diagram for explaining a read operation of the semiconductor memory device according to the present invention.

FIG. 9 is a block diagram of a semiconductor memory device

according to another embodiment of the present invention.

FIG. 10 is a circuit diagram showing a portion of a row decoder & driving block shown in FIG. 9.

Description of the Preferred Embodiment

A circuit diagram of a semiconductor integrated circuit device according to the present invention will now be described with reference to FIG. 1.

Referring to FIG. 1, a semiconductor integrated circuit 10 outputs an output signal OUT in response to input signals IN1 and IN2 and includes a first internal circuit 12, a second internal circuit 14, and an interface circuit 16. The first internal circuit 12 operates with a higher voltage VPP than an internal power supply voltage IVC (or external power supply voltage EVC), while the second internal circuit 14 and the interface circuit 16 operate with the internal power supply voltage IVC (or the external power supply voltage EVC). The internal power supply voltage IVC has the same level as the external power supply voltage EVC. Alternatively, the internal power supply voltage IVC has a lower level than the external power supply voltage EVC. The interface circuit 16 limits a voltage that is applied from the first internal circuit 12 to the second internal circuit 14 or applied from an output terminal OUT to the second internal circuit 14. The interface circuit 16 acts as voltage-limiting means.

The first internal circuit 12 includes a POMS transistor MP1 having a relatively thick gate insulation layer so as to have a sufficient withstand voltage relative to a high voltage VPP. The PMOS transistor MP1 is coupled to enable its gate to receive an input signal IN1 and has a source coupled to

a power terminal receiving the high voltage VPP and a drain coupled to the output terminal OUT. The interface circuit 16 includes an NMOS transistor MN1 having a relatively thin gate insulation layer so as to have a withstand voltage relative to the IVC/EVC voltage. The NMOS transistor MN1 has a gate coupled to the IVC/EVC voltage, a drain coupled to the output terminal OUT, and a source. The second internal circuit 14 includes an NMOS transistor MN2 having a relatively thin gate insulation layer so as to have a withstand voltage relative to the IVC/EVC voltage. The NMOS transistor MN2 is coupled to enable its gate to receive an input signal IN2 and has a drain coupled to the source of the NMOS transistor MN1 and a source coupled to a ground voltage VSS.

The input signal IN1 selectively has a ground voltage VSS and a high voltage VPP. The input signal IN2 selectively has a ground voltage VSS and an internal power supply voltage IVC (or external power supply voltage EVC).

The NMOS transistor MN1 of the interface circuit 16 prevents a high voltage supplied through a PMOS transistor MP1 from being directly applied to the drain of the NMOS transistor MN2. That is, since a voltage of the output terminal OUT is transferred through the NMOS transistor MN1 whose gate is coupled to the IVC/EVC voltage, a voltage of IVC/EVC-Vtn1 is applied to the drain of the NMOS transistor MN2, instead of the high voltage VPP. Here the Vtn1 means a threshold voltage of an NMOS transistor having a relatively thin gate insulation layer. Since the IVC/EVC is always applied to the gate of the NMOS transistor MN1, a gate-drain voltage difference of the NMOS transistor MN1 is VPP-IVC/EVC. Therefore, although the NMOS transistor MN1 has the relatively thin gate insulation layer, a gate insulation

layer of the NMOS transistor MN1 is not broken by the high voltage VPP.

If the NMOS transistor MN1 is not used, the gate-drain voltage difference Vgd1 of the NMOS transistor MN2 is the VPP voltage maximally, as shown in FIG. 2. This means that, in a case where the NMOS transistor MN2 having a relatively thin gate insulation layer is used, the gate insulation layer of the NMOS transistor MN2 is broken. Thus, the NMOS transistor MN2 must have a relatively thick gate insulation layer. In this case, the input signal IN2 of the NMOS transistor MN2 must have a high voltage VPP during an active state. If not so, the turn-on speed of the NMOS transistor MN2 is relatively lowered. On the other hand, when the NMOS transistor MN1 is used, a gate-drain voltage difference Vgd2 of the NMOS transistor MN2 is the IVC voltage maximally (when IVC is lower than EVC), as shown in FIG. 2. When the IVC is equivalent to the EVC), the gate-drain voltage difference Vgd2 of the NMOS MN2 is IVC-Vtnh. That is, an electric field applied to the gate insulation layer of the NMOS transistor MN2 is alleviated. Therefore, the NMOS transistor MN1 for interface (or attenuating an electric field) is constructed between the internal circuits 12 and 14 to prevent the gate insulation layer of the NMS transistor MN2 from being broken by applying a high voltage to a drain as well as to prevent the turn-on speed of the NMOS transistor MN2 from being lowered.

Another embodiment of semiconductor integrated circuit devices according to the present invention is illustrated in FIG. 3.

Referring to FIG. 3, a semiconductor integrated circuit device 20 includes a first internal circuit 22, a second internal circuit 24, an interface circuit 26, and an inverter INV1. The interface circuit 26 limits a voltage applied from the first internal circuit 22 to the second internal circuit 24 and

acts as voltage-limiting means (or field-alleviating means). The first internal circuit 22 includes PMOS transistors MP2 and MP3 with a relatively thick gate insulation layer so as to have a sufficient withstand voltage relative to a high voltage VPP. The PMOS transistor MP2 has a source coupled to the high voltage VPP, a drain coupled to an internal node ND1, and a gate coupled to receive an input signal IN1. The input signal IN1 selectively has a high voltage VPP and a ground voltage VSS. The PMOS transistor MP3 has a source coupled to the high voltage VPP, a drain coupled to the internal node ND1, and a gate coupled to an output terminal OUT.

The interface circuit 26 includes an NMOS transistor MN3 with a relatively thin gate insulation layer so as to have a sufficient withstand voltage relative to an internal power supply voltage IVC or an external power supply voltage EVC. The NMOS transistor MN3 has a gate coupled to an internal power supply voltage IVC or an external power supply voltage EVC, a drain coupled to an internal node ND1, and a source coupled to a second internal circuit 24. The second internal circuit 24 includes NMOS transistors MN4, MN5, MN6, and MN7 with a relatively thin gate insulation layer so as to have a sufficient withstand voltage relative to an internal power supply voltage IVC or an external power supply voltage EVC. The NMOS transistors MN4-MN7 are serially coupled between an interface circuit 26, i.e., a source of the NMOS transistor MN3 and a ground voltage VSS and are controlled by corresponding input signals IN2, IN3, IN4, and IN5 respectively. Each of the input signals IN2-IN5 has an internal power supply voltage IVC or an external power supply voltage EVC in an active state and has a ground voltage VSS in an inactive state. An inverter INV1 is coupled between an internal node ND1 and an output terminal OUT and

includes PMOS and NMOS transistors MP4 and MN8. Each of the transistors MP4 and MN8 has a relatively thick gate insulation layer so as to a sufficient withstand voltage relative to a high voltage VPP. The PMOS and NMOS MP4 and MN8 are serially coupled between a high voltage VPP and a ground voltage VSS. Gates of the PMOS and NMOS transistors MP4 and MN8 are commonly connected to an internal node ND1.

The operation of the semiconductor integrated circuit device according to the present invention will now be described hereinbelow.

When an input signal IN1 has a low level of a ground voltage VSS and at least one of input signals IN2-IN5 has a low level of a ground voltage VSS, an internal node ND1 are precharged to a high voltage VPP through a PMOS transistor MP2. In this case, an output signal OUT becomes a low level of a ground voltage VSS, so that a PMOS transistor is also turned on. Since an NMOS transistor MN3 having a gate coupled to an internal power supply voltage IVC or an external power supply voltage EVC is always in a turn-on state, a voltage of IVC-Vtnl is applied to a drain of an NMOS transistor MN4 through an NMOS transistor MN3. That is, a voltage applied to the drain of the NMOS transistor MN4 is restricted by an NMOS transistor MN3 of an interface circuit 26. Accordingly, although an NMOS transistor MN4 has a relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN4 is not broken by the high voltage VPP without lowering a turn-on speed. Similarly, since IVC/EVC is always applied to the gate of the NMOS transistor MN3, a gate-drain voltage difference of an NMOS transistor is VPP-IVC/EVC. Although the NMOS transistor MN3 has a relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN3 is not broken by a high voltage VPP. When an input signal

IN1 has a high level of a high voltage VPP and input signals IN2-IN5 have a high level of IVC/EVC, a voltage of an internal node ND1 is discharged through an interface circuit 26 and a second internal circuit 24, i.e., NMOS transistors MN3-MN7. The output signal OUT has a high level through an inverter INV1.

Another embodiment of the semiconductor integrated circuit device according to the invention will now be described with reference to FIG. 4.

Referring to FIG. 4, a semiconductor integrated circuit device 30 includes a first internal circuit 32, a second internal circuit 34, and an interface circuit 36.

The first internal circuit 32 includes PMOS transistors MP5 and MP6 with a relatively thick gate insulation layer so as to have a sufficient withstand voltage relative to a high voltage VPP. The PMOS transistor MP5 has a source coupled to a high voltage VPP, a drain coupled to an internal node ND2, and a gate coupled to an internal node ND3. The PMOS transistor MP6 has a source coupled to a high voltage VPP, a drain coupled to an internal node ND3, and a gate coupled to an internal node ND2.

The second internal circuit includes NMOS transistors MN11 and MN12 and an inverter INV2 and operates with an internal power supply voltage IVC or an external power supply voltage EVC. Each of the NMOS transistors MN11 and MN12 has a relatively thin gate insulation layer so as to have a sufficient withstand voltage relative to an internal power supply voltage IVC or an external power supply voltage EVC. The NMOS transistor MN11 has a drain coupled to an internal node ND4, a source coupled to a ground voltage VSS, and a gate connected to receive an input signal IN. The NMOS transistor MN12 has a drain coupled to an internal node ND5, a

source coupled to a ground voltage VSS, and a gate connected to receive an inverted input signal INB through an inverter INV2. The inverter INV2 operates with an internal power supply voltage IVC or an external power supply voltage EVC and includes PMOS and NMOS transistors (not shown) with a relatively thin gate insulation layer.

The interface circuit 36 reduces an electric field applied to a gate insulation layer of NMOS transistors MN11 and MN12 and restricts a voltage applied from the internal node ND2 or ND3 to the second internal circuit 34. The interface circuit 36 includes NMOS transistors MN9 and MN10 with a relatively thin gate insulation layer so as to have a sufficient withstand voltage relative to an internal power supply voltage IVC or an external power supply voltage EVC. The NMOS transistor MN9 is coupled between internal nodes ND2 and ND4, and the NMOS transistor MN10 is coupled between internal nodes ND3 and ND5. Gates of NMOS transistors MN9 and MN10 are commonly coupled to an internal power supply voltage IVC or an external power supply voltage EVC.

The operation of the semiconductor integrated circuit device according to this embodiment will now be described in detail.

When an input signal IN has a low level, an NMOS transistor MN11 is turned off and an MOS transistor MN12 is turned on. Since an ND3 node goes to a low level through NMOS transistors MN10 and MN12, a PMOS transistor MP5 is turned on and an output signal goes to a high level of a high voltage VPP. When the input signal has a high level, the NMOS transistor MN13 is turned off and the NMOS transistor MN11 is turned on. Since an ND2 node goes to a low level through the NMOS transistors MN9 and MN11, a PMOS transistor MP6 is turned on and an output signal OUT

goes to a low level of a ground voltage VSS.

Since each of NMOS transistors MN9 and MN10 has a gate coupled to an internal power supply voltage IVC and an external voltage is always turned on, a voltage of IVC/EVC-Vtnl is applied to an NMOS transistor MN11 or MN12 through the NMOS transistor MN9 or MN10. That is, a voltage applied to a drain of an NMOS transistor MN11 or MN12 is restricted by the NMOS transistor MN9 or MN10 of the interface circuit 36. Accordingly, although each of the NMOS transistors MN11 and MN12 has a relatively thin gate insulation layer, the gate insulation layers of the NMOS transistors MN11 and MN12 are not broken by the high voltage VPP. Further, since each of the NMOS transistors MN11 and MN12 has the relatively thin gate insulation layer, the turn-on speed of the NMOS transistors MN11 and MN12 is not reduced. Likewise, since IVC/EVC is always applied to the gates of the NMOS transistors MN9 and MN10, a gate-drain voltage difference of the respective NMOS transistors MN9 and MN10 is VPP-IVC/EVC. Although the NMOS transistor MN9 and MN10 have the relatively thin gate insulation layer, the gate insulation layers of the NMOS transistors MN9 and MN10 are not broken by a high voltage VPP.

A block diagram of a semiconductor memory device employing the semiconductor integrated circuit device according to the present invention is illustrated in FIG. 5.

Referring to FIG. 5, a semiconductor memory device 100 includes a memory cell array 110 having a plurality of memory blocks MB0, MB1, ..., and MBy. Each of the memory blocks MB0, MB1, ..., and MBy includes memory cells disposed in a matrix of rows (or wordlines) or columns (bitlines). A row predecoder 120 generates decoding signals DRAi[0:m],

DRAj[0:n], and DRAk[0:x] and block selecting signals BLK[0:y]. The block selecting signals BLK[0:y] correspond to the memory blocks MB0-MBy, respectively. The decoding signals DRAi[0:m], DRAj[0:n], and DRAk[0:x] are used to select one of the wordlines of a selected memory block.

The semiconductor memory device 100 includes level shift blocks LSB0, LSB1, ..., and LSBy each corresponding to memory blocks MB0-MBy. Each of the level shift blocks LSB0-LSBy inputs a corresponding a block selecting signal and decoding signals DRAk[0:x]. For example, the level shift block LSB0 inputs the block selecting signal BLK0 and the decoding signals DRAk[0:k], the level shift block LSB1 inputs the block selecting signal BLK1 and the decoding signals DRAk[0:k], and the level shift block LSBy inputs the block selecting signal BLKy and the decoding signals DRAk[0:k]. Input signals of the level shift blocks LSB0-LSBy each have an internal power supply voltage IVC or an external power supply voltage EVC during the active state. The level shift blocks LSB0-LSBy output decoding signals including block selecting information in response to the input signals. For example, the level shift block LSB1 outputs decoding signals DRA1k[0:x] in response to input signals, and the level shift block LSBy outputs decoding signals DRAyk[0:x] in response to input signals.

The semiconductor memory device 100 further includes row decoder and driver blocks 130_0, 130_1, ..., and 130_y each corresponding the memory blocks MB0, MB1, ..., and MBy. The row decoder and driver blocks 130_0, 130_1, ..., and 130_y operate with a high voltage VPP. Each of the row decoder and driver circuits 131 drives a corresponding wordline in response to a part of the decoding signals DRAi[0:m] and DRAj[0:n] from the row predecoder 120 and a part of the decoding signals (e.g., DRA0k[0:x]

from a corresponding level shift block (e.g., LSB0).

The level shift blocks and row decoder and the driving blocks according to the present invention are implemented using the dual circuit device of the dual insulation system described in FIG. 1, FIG. 3, and FIG. 4. This will now be described hereinbelow more fully. As shown in FIG. 5, outputs signals of the respective level shift blocks are inputted only to their corresponding memory blocks to reduce power consumption.

FIG. 6 is a circuit diagram showing a part of the level shift block shown in FIG. 5. A level shift circuit LS shown in FIG. 6 is one of the level shift circuits of the level shift block each corresponding to decoding signals DRAk0-DRAkx. The other level shift circuits have the same construction as the level shift circuit LS shown in FIG. 6. The level shift circuit LS shown in FIG. 6 outputs a decoding signal DRA0k0 in response to a decoding signal DRAk0 and a block selecting signal BLK0. The decoding signal DRAk0 and the block selecting signal BLK0 have an internal power supply voltage IVC or an external power supply voltage EVC during the active state, and the decoding signal DRA0k0 has a high voltage VPP during the active state. The level shift circuit LS includes two PMOS transistors MP20 and MP21, four NMOS transistors MN20, MN21, MN22, and MN23, an inverter INV20, and a NAND G20.

Each of the PMOS transistors MP20 and MP21 has a relatively thick gate insulation layer so as to have a sufficient withstand voltage relative to a high voltage, while each of the NMOS transistors MN20-MN23 has a relatively thin gate insulation layer so as to have a sufficient withstand voltage relative to an internal power supply voltage IVC or an external power supply voltage EVC. Although not shown in this figure, NMOS

transistors constituting the NAND gate G20 and the inverter INV20 have a relatively thin gate insulation layer so as to have a sufficient withstand voltage relative to an internal power supply voltage IVC or an external power supply voltage EVC.

The PMOS transistor MP20 has a gate coupled to ND21, a source coupled to a high voltage VPP, and a drain coupled to ND20 (output terminal DRA0k0). The PMOS transistor MP21 has a gate coupled to ND20, a source coupled to a high voltage VPP, and a drain coupled to ND21. The NMOS transistors MN20 and MN22 are serially coupled between ND20 and a ground voltage VSS. The NMOS transistors MN21 and MN23 are serially coupled between ND21 and a ground voltage VSS. Gates of the MOS transistors MN20 and 21 are connected to an internal power supply voltage IVC and an external power supply voltage EVC. The NMOS transistor MN22 is controlled by a clock signal NOUT of an NAND gate G20 operating in response to the decoding signal DRAk0 and the block selecting signal BLK0. The inverter INV20 inverts an output signal of the NAND gate G20. The NMOS transistor MN23 is controlled by an output signal of the inverter INV20.

The operation of the level shift circuit shown in FIG. 6 will now be described hereinbelow more fully.

When at least one of the decoding signal DRA0k and the block selecting signal BLK0 has a low level, the NMOS transistor MN22 is turned on and the NMOS transistor MN23 is turned off. Accordingly, the ND20 has a low level through the NMOS transistors MN20 and MN22. As the PMOS transistor MP21 is turned on, the ND21 has a high voltage VPP and the PMOS transistor MP20 is turned off. Although the ND21 has the high

voltage VPP, the NMOS transistors MN21 and MN23 each having the relatively thin gate insulation layer are not affected by the high voltage VPP. This is because a gate-drain voltage difference of the NMOS transistor MN21 having a gate coupled to IVC/EVC is VPP-IVC/EVC and a gate-drain voltage difference of the NMOS transistor MN23 is IVC/EVC-Vtnl.

When the decoding signal DRA0k and the block selecting signal BLK0 have a high level, the NMOS transistor MN22 is turned off and the NMOS transistor MN23 is turned on. Accordingly, the ND21 has a low level through the NMOS transistors MN21 and MN23. As the PMOS transistor MP20 is turned on, the ND20 has a high voltage VPP and the PMOS transistor MP21 is turned off. An output signal DRA0k0 including block selecting information has a high voltage VPP. Although the ND20 has the high voltage VPP, the NMOS transistors MN20 and MN22 each having the relatively thin gate insulation layer are not affected by the high voltage VPP. This is because a gate-drain voltage difference of the NMOS transistor MN20 having a gate coupled to IVC/EVC is VPP-IVC/EVC and a gate-drain voltage difference of the NMOS transistor MN22 is IVC/EVC-Vtnl.

In this embodiment, the PMOS transistors MP20 and MP21 constitute a first internal circuit operating with a high voltage VPP. The NAND gate, the inverter INV20, and the NMOS transistors MN22 and MN23 constitute a second internal circuit operating with an internal power supply voltage IVC and an external power supply voltage EVC. The NMOS transistors MN20 and MN21 constitute means for restricting a voltage transmitted from the first internal circuit to the second internal circuit.

FIG. 7 is a circuit diagram showing a part of the row decoder and driver block shown in FIG. 5. A row decoder and driver circuit 131 shown in

FIG. 7 is coupled to one of wordlines each corresponding to the row decoder and driver blocks 130_0~130_y. Row decoder and driver circuits each being coupled to the other wordlines have the same construction as the row decoder and driver circuit shown in FIG. 7. The circuit 131 drives a corresponding wordline in response to decoding signals (e.g., DRA0k0, DRAi0, and DRAj0). The decoding signal DRA0k0 is inputted from a corresponding level shift block and has a high level of a high voltage during the active state. The decoding signals DRAi0 and DRAj0 are inputted from the row predecoder 120 shown in FIG. 5 and have an internal power supply voltage IVC or an external power supply voltage EVC during the active state.

Referring to FIG. 7, the row decoder and driver circuit 131 includes PMOS transistors MP22, MP23, and MP24 and NMOS transistors MN24, MN25, MN26, and MN27. The PMOS transistor having a gate connected to receive a control signal P_0 has a source coupled to a high voltage VPP and a drain coupled to an internal node ND22. The NMOS transistors MN24-MN26 are serially coupled between the internal node ND24 and a ground voltage VSS, and are controlled by decoding signals DRA0k0, DRAi0, and DRAj0, respectively. The PMOS transistor MP23 has a gate coupled to an output terminal ND24, a source coupled to a high voltage VPP, and a drain coupled to an internal node ND23. The PMOS and NMOS transistors MP24 and MN27 constitute an inverter and are coupled between the internal node ND22 and the output terminal ND24 (i.e., a wordline WL).

The operation of the row decoder and driver circuit 131 will now be described hereinbelow more fully.

When the control signal P_0 has a low level and at least one of the decoding signals DRA0k0, DRAi0, and DRAj0 has a low level, a current

path between the internal node ND22 and the ground voltage VSS is cut off and a current path is formed between the internal node ND22 and the ground voltage VSS. Accordingly, the wordline WL is driven with the high voltage VPP through the PMOS transistor MP24. As described above, since the high voltage VPP of the node ND22 is transmitted through the NMOS transistor MN24 as interface means, a gate insulation layer of the NMOS transistor is not affected by the high voltage VPP.

The operation of the semiconductor memory device according to the invention will now be described with reference to a timing diagram of FIG. 8.

When a control signal P_0 and decoding signals DRAykx, DRAim, and DRAjn have a high level, the PMOS transistor MP22 shown in FIG. 7 is turned on and the NMOS transistors MN24-MN26 shown in FIG. 7 are turned off. Accordingly, wordlines go to a low level. As shown in FIG. 8, as the control signal P_0 goes to a high level, the PMOS transistor shown in FIG. 7 is turned off. Block selecting signals BLK[0:y] and decoding signals DRAk[0:x] are inputted to corresponding level shift blocks LSB0-LSBj. A level shift block corresponding to a selected memory block shifts a voltage level of decoding signals having a high level of IVC/EVC to a high voltage VPP. As shown in FIG. 8, high-level decoding signals outputted from the level shift block have a high voltage VPP, instead of an internal power supply voltage IVC or an external power supply voltage EVC, through corresponding level shift circuits (see FIG. 6). Thereafter, one of the row decoder and driver circuits in a selected memory block operates a wordline WL with a high voltage VPP in response to the input signals DRAykx, DRAim, and DRAjn.

As previously stated, a MOS transistor (NMOS transistor MN24 of

FIG. 7) having a relatively thick gate insulation layer is used for preventing a gate insulation layer from being broken by a high voltage in an integrated circuit employing a dual insulation system. In the case where a voltage applied to the gate of the NMOS transistor MN24 is an internal power supply voltage IVC or an external power supply voltage EVC, the high voltage VPP of the node ND22 shown in FIG. 7 is discharged along a dotted line of FIG. 8. This is because it is difficult to sufficiently turn on the NMOS transistor having the relatively thick gate insulation layer by using IVC/EVC. As a result, the activation speed of the wordline WL is lowered.

In case of the semiconductor memory device according to the invention, however, the gate voltage of the NMOS transistor MN24 is set to a high voltage to turn on the NMOS transistor MN24 having the relatively thick gate insulation layer in a sufficiently high speed. Thus, a discharge speed of the ND22 voltage of the row decoder and driver circuit 131 makes higher by tD, as shown in FIG. 8. As a result, the activation speed of the wordline WL becomes higher by tD.

FIG. 9 is a block diagram of a semiconductor memory device according to another embodiment of the present invention, and FIG. 10 is a circuit diagram showing a portion of a row decoder & driving block shown in FIG. 9.

Unlike the row decoder and driver blocks shown in FIG. 5, row decoder and driver blocks 130'_0~130'_y shown in FIG. 10 receive output signals of a row predecoder 120' as their entirety. Row decoder and driver blocks shown in FIG. 10 have a dual insulation system so as to operate with a high voltage VPP and an internal power supply voltage IVC or an external power supply voltage EVC. This will now be described more fully with

reference to FIG. 10.

Referring to FIG. 10, a row decoder and driver block 131' coupled to any wordline drives a wordline WL with a high voltage VPP in response to decoding signals DRAim, DRAjn, DRAkx, and BLKy. Each of the decoding signals has an internal power supply voltage IVC or an external power supply voltage EVC during the active state. The semiconductor memory device shown in FIG. 9 adopts only the interface manner shown in FIG. 3, not using the level shift block.

The row decoder and driver circuit 131' includes PMOS transistor P25, MP26, and MP27 and the NMOS transistors MN28, MN29, MN30, MN31, MN32, and MN33. Each of the transistors MP25, MP26, MP27, and MN33 has a relatively thick gate insulation layer, and each of the transistors MN28-MN32 has a relatively thin gate insulation layer. The PMOS transistors MP25 and MP26 constitute a first internal circuit operating with a high voltage VPP, and the NMOS transistors MN29-MN32 constitute a second internal circuit operating with an internal power supply voltage IVC or an external power supply voltage EVC. The NMOS transistor MN28 acts as an interface circuit (or voltage restricting means) for restricting a voltage applied from the first internal circuit to the second internal circuit. The row decoder and driver circuit shown in FIG. 10 operates the same as the integrated circuit device shown in FIG. 3, which will not be explained in further detail.

As described above, since the high voltage VPP of the node ND25 is transmitted to the drain of the NMOS transistor MN29 through the NMOS transistor MN28, a gate-drain voltage difference of the NMOS transistor MN29 is IVC/EVC-Vtnl. Thus, although the NMOS transistor MN29 has a

relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN29 is not affected by the high voltage VPP. Since IVC/EVC is always applied to the gate of the NMOS transistor MN28, a gate-drain voltage difference of the NMOS transistor is VPP-IVC/EVC. Although the NMOS transistor MN28 has a relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN28 is not broken by the high voltage VPP.

In the invention, IVC/EVC is applied to a MOS transistor constituting an interface circuit. However, a gate voltage of the MOS transistor constituting the interface circuit may be variously regulated within a scope where a relatively thin gate insulation layer is not affected. For example, a voltage between an internal (or external) power supply voltage and a high voltage or a voltage between an internal (or external) power supply voltage and a ground voltage may be used.

While the present invention has been set forth and described with respect to two rather specific embodiments, it will be appreciated that other and different systems could readily be designed by those skilled in the art, without significantly departing from the spirit and scope of the invention.